WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a projecting second semiconductor layer which is formed on a first semiconductor layer;

third and fourth semiconductor layers which are formed on the first semiconductor layer to be in contact with the second semiconductor layer and oppose each other via the second semiconductor layer;

a gate electrode which is in contact with the second semiconductor layer with a gate insulating film interposed therebetween and forms a channel in the second semiconductor layer; and

an insulating film which is formed in the first semiconductor layer located immediately under the third and fourth semiconductor layers.

2. The device according to claim 1, wherein the insulating film is formed in the first semiconductor layer to surround a region located immediately under the second semiconductor layer.

3. The device according to claim 1, wherein the third and fourth semiconductor layers are isolated from the first semiconductor layer by the insulating film.

4. The device according to claim 1, wherein the gate electrode is formed so its ends oppose each other via the second semiconductor layer in a direction perpendicular to a direction in which the third and fourth semiconductor layers oppose each other.

5. The device according to claim 1, further comprising a cell capacitor which is formed on the first semiconductor layer and whose storage node electrode is connected to one of the third and fourth semiconductor layers.

6. The device according to claim 5, wherein the cell capacitor comprises

a trench which is formed in the first semiconductor layer,

the storage node electrode which fills the trench with a capacitor insulating film interposed therebetween, and

a plate electrode which is formed in a region around the trench in the first semiconductor layer.

7. A semiconductor device comprising:

an insulating film formed on a first semiconductor layer;

a projecting second semiconductor layer which is formed on the insulating film;

third and fourth semiconductor layers which are formed on the insulating film to be in contact with the second semiconductor layer and oppose each other via the second semiconductor layer;

a gate electrode which is in contact with the second semiconductor layer with a gate insulating film interposed therebetween and forms a channel in the second semiconductor layer; and

a connection region which is formed immediately under the second semiconductor layer to electrically connect the first semiconductor layer and the second semiconductor layer.

8. The device according to claim 7, wherein the connection region is isolated from the third and fourth semiconductor layers by the insulating film.

9. The device according to claim 7, wherein in the connection region, the insulating film in a partial region immediately under the second semiconductor layer is removed, and a fifth semiconductor layer is formed in the region where the insulating film is removed.

10. The device according to claim 7, wherein the third and fourth semiconductor layers are isolated from the first semiconductor layer by the insulating film.

11. The device according to claim 7, wherein the gate electrode is formed so its ends oppose each other via the second semiconductor layer in a direction perpendicular to a direction in which the third and fourth semiconductor layers oppose each other.

12. The device according to claim 7, further comprising a cell capacitor which is formed on the first semiconductor layer and whose storage node electrode is connected to one of the third and fourth semiconductor layers.

13. The device according to claim 12, wherein the cell capacitor comprises

a trench which is formed in the first semiconductor layer,

the storage node electrode which fills the trench via a capacitor insulating film, and

a plate electrode which is formed in a region around the trench in the first semiconductor layer.

14. A method for fabricating a semiconductor device, comprising:

forming a first insulating film on a first semiconductor layer;

making a hole that reaches the first semiconductor layer in the first insulating film;

forming a second semiconductor layer on the first insulating film and in the hole;

patterning the second semiconductor layer into a columnar shape to make part of the second semiconductor layer cover the hole;

forming a gate insulating film on a side surface of the second semiconductor layer;

forming a third semiconductor layer on the gate insulating film and first insulating film;

patterning the third semiconductor layer and leaving the third semiconductor layer on a side surface of the second semiconductor layer in a region that should be a channel region to form a gate electrode; and

forming source and drain regions in a region of

the second semiconductor layer located on the first insulating film.

15. A method according to claim 14, further comprising

after forming the hole, forming a second insulating film on the first insulating film and in the hole not to completely fill the hole, and

partially removing the second insulating film to expose the first semiconductor layer to a bottom portion of the hole while leaving the second insulating film on a sidewall of the hole.

16. The method according to claim 14, further comprising:

after forming the second semiconductor layer, making a trench that reaches from the second semiconductor layer to the first semiconductor layer;

forming a plate electrode in a partial region in the first semiconductor layer around the trench;

forming a capacitor insulating film on an inner wall of the trench; and

forming a storage node electrode in the trench to fill the trench, and

after forming the source and drain regions, forming a contact plug which electrically connects the source region and the storage node electrode,

wherein, in patterning the second semiconductor layer into a columnar shape, the second semiconductor

layer is patterned such that a region where the source region is to be formed in the second semiconductor layer into contact with the trench.

17. A method for fabricating a semiconductor device, comprising:

making a hole in a substrate prepared by sequentially forming a first insulating film and second semiconductor layer on a first semiconductor layer, the hole extending through the second semiconductor layer and the first insulating film to expose the first semiconductor layer to a bottom portion of the hole;

forming a third semiconductor layer on the second semiconductor layer and in the hole;

patterning the second and third semiconductor layers into a columnar shape to make part of the third semiconductor layer cover the hole;

forming a gate insulating film on a side surface of the second and third semiconductor layers;

forming a fourth semiconductor layer on the gate insulating film and first insulating film;

patterning the fourth semiconductor layer and leaving the fourth semiconductor layer on a side surface of the second and third semiconductor layers in a region that should be a channel region to form a gate electrode; and

forming source and drain regions in a region of the second and third semiconductor layers located on

the first insulating film.

18. The method according to claim 17, further comprising

after making the hole, forming a second insulating film on the second semiconductor layer and in the hole not to completely fill the hole, and

partially removing the second insulating film to expose the first semiconductor layer to a bottom portion of the hole while leaving the second insulating film on a sidewall of the hole.

19. The method according to claim 17, further comprising:

after forming the third semiconductor layer, forming a trench that reaches from the third semiconductor layer to the first semiconductor layer;

forming a plate electrode in a partial region in the first semiconductor layer around the trench;

forming a capacitor insulating film on an inner wall of the trench; and

forming a storage node electrode in the trench to fill the trench, and

after forming the source and drain regions, forming a contact plug which electrically connects the source region and the storage node electrode,

wherein, in patterning the second and third semiconductor layers into a columnar shape, the second and third semiconductor layers are patterned such that

a region where the source region is to be formed in the second and third semiconductor layers into contact with the trench.